APPLICATION NOTE

Inductive Load Test Losses

Purpose

This application note describes the major losses that occur when using an external inductive load box. Some of these losses are due to the switching components needed to select multiple inductance values.

Losses In Inductive Load Testing

During the early years when Unclamped Inductive Switching (UIS) testing was first beginning to be used as a production test for MOSFET ruggedness, the product mix was predominantly medium to high voltage (100-600V) devices, with a single die per package.

The ITC5510 Series testers and the ITC5514A,B Inductive Load Boxes, developed by ITC, used relay contact switching to handle polarity and inductor value changes, because rapid switching to accommodate multi-die configurations wasn't required. As a result, the losses in the load circuit of the DUT were negligible.

In more recent years, low voltage (<50 V) devices, often with multiple die, are being manufactured in large quantities. For this reason ITC developed its latest series of UIS testers (ITC55x00) and Inductive Load Boxes (ITC55140)use solid state switching to enhance the reliability and testing speed for multi-die packages.

These factors combined may cause the losses during testing to become quite significant. The nature of these losses and the new "Compensated" mode of operation which corrects for these losses are discussed below.

Basic Theory Of UIS Testing Reviewed

A simplified schematic of the UIS tester is shown in Figure-1. At the onset of the test, switch S1 is closed and the gate of the DUT is energized, creating a series loop consisting of the drain power supply, the load inductor, and the DUT. The current in the loop will rise in a linear manner (T1 period). When the current reaches the setpoint, switch S1 opens, switch S2 closes, and the DUT is turned off by lowering the gate voltage to 0 volts.

Current in the inductor continues to flow and causes the voltage across the DUT to rise until the avalanche breakdown voltage is reached. The device begins conducting in avalanche and dissipates the energy that was stored in the inductor. The current decays in a linear fashion (T2 period) until the energy is fully depleted.

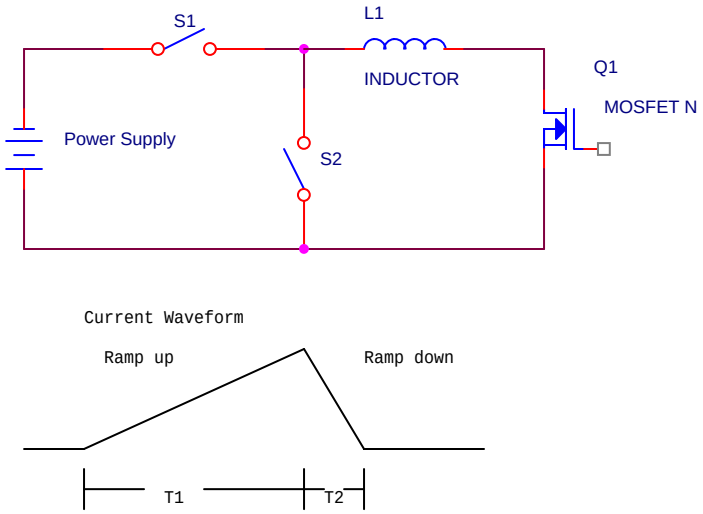

Figure 1: Simplifed Ideal Test UIS Diagram

In this "ideal" case, with no losses, the relation ship between current, voltage, inductance, and time is given as:

$$\text{Time} = \frac{\text{Induc tan ce} * \text{Current}}{\text{Voltage}}$$

The energy stored in the inductor during the T1 half of the test, as well as the energy dissipated by the DUT during the T2 half of the test, is given as:

$$\text{Time} = \frac{\text{Induc tan ce} * \text{Current}^2}{\text{Voltage}}$$

When testing medium to high voltage devices at moderate currents with the first generation of UIS testing equipment, these simplified equations are sufficiently accurate.

Compare the situation depicted in Figure-2, where resistance and conduction losses are considered. The lower potion of Figure-2 shows the effect on the current waveform and the time relationships. The "ideal" waveform is shown dotted for reference.

NOTE: The linear ramps have become curved, and the time to reach the setpoint current has increased, while the time for the energy to be dissipated has decreased.

The energy the DUT dissipates is now less than the energy that was "stored" in the inductor. This can be easily visualized if you consider that the energy received by the DUT is the instantaneous product of the decaying current waveform and the DUT avalanche voltage summed over the duration of the decay. If two DUTs of equal voltage

rating were placed in series, then the energy received by each one would be half of the total energy stored in the inductor. Likewise, any voltage drops in the loop will receive a portion of the energy, thus depriving the DUT of the energy that was intended for it.

In the case of essentially constant voltage drops (forward conduction losses), the energy received by the DUT will be proportional to the ratio of its B_{vdss} to the sum of its B_{vdss} and the other voltage drops in the loop. In the case of loop resistance, the situation is more complicated because its voltage drop varies with the current as it decays. The presence of resistance is what causes the curvature of the current ramps seen in the diagram.

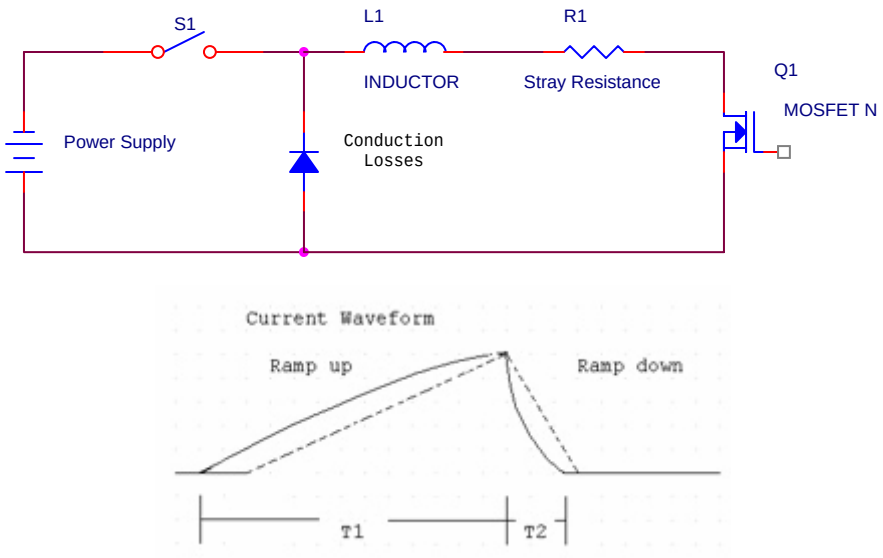

Figure 2: Simplifed Typical UIS Test Diagram

Compensation For Losses

The effect of the losses, previously discussed, can be compensated so that they do not affect the testing results. Previously, this needed to be done by testing and monitoring the current and voltage waveforms across the DUT. The energy delivered to the DUT could be determined from these waveforms, then adjustments to the peak current or inductor size could be made. Changing these values, of course, alters the losses in the circuit. A second iteration might need be done to get a satisfactory result.

New equations developed for use in the ITC55X00 series of USI testers can be used by selecting the “compensated” mode. These equations do the “fine tuning” for the user by taking into account the resistive and forward conduction losses in both the tester and the inductive load box.

Data tables stored in the program hold all of these values for the ITC series of inductive load boxes as well as for the ITC55X00 testers. These values are used to correct the ramp up time (T1), ramp down time (T2), and the DUT energy values so that departures from “ideal” behavior can be taken into account.

Compatibility with previously established test setups is maintained by using the “original” mode. This mode utilizes all of the previous equations so the test will be conducted as it has been in the past.